REMARKS

Claims 25, 27-32, 34-37, 39-50, 52 and 53 are pending in the present application. Claims 26 and 51 have been withdrawn from consideration. By this amendment, independent claims 29, 52 and 53 have been amended. In light of the amendments above and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Claims 25, 27-32, 34-37, 45-50 and 52-53 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuzaki et al. (U.S. Pat. No. 6,500,715; hereinafter "Matsuzaki).[1] Applicants have amended independent claims 29, 52 and 53 to recite "wherein the pulse generator circuit is configured such that the flip-flop input signal is precharged to a first electrical potential during a precharging clock signal phase, that the flip-flop input signal is brought to a second electrical potential by a rising clock edge following the precharging clock signal phase, and that the state of the flip-flop input signal can no longer be altered after the rising clock edge." Support for these amendments can be found at least in Figure 3 and paragraph [0093] of the published patent application (U.S. Pat. Pub. No. 2006/0084236 A1).

The Office Action contends the Matsuzaki's NAND gate (NA1) reads on the "pulse generator circuit" limitation of the present invention. The state of NAND gate NA1 is controlled by the signal level of timing signal ϕ. Thus, when ϕ is at "H" (high level), NA1 is on and provides the output signal "Ai NAND Aj" as the input signal to inverter IV1, which in turn provides the inverted signal as the input signal to the level holder circuit LH1. Moreover, when ϕ is at "L" (low level), NA1 is off and the output signal of NA1 is floating. As long as NA1 is in the on-state (ϕ = "H"), it is transparent to any change in Ai and Aj, meaning that whenever signals Ai and/or Aj change their states during the on-state of NA1, the state of the output signal of NA1 (and consequently of the input signal provided to LH1) may change accordingly. In other words, during the on-state of NA1,

[1] The Office Action does not indicate at page 2 that claim 32 is rejected as being anticipated by Matsuzaki, but it clearly is rejected as discussed at page 4.

the state of the input signal provided to the level holder circuit LH1 may change an arbitrary number of times.

In contrast, amended claims 29, 52 and 53 require that the pulse generator circuit is configured such that the state of the flip-flop input signal may change from a first electrical potential (during a precharging phase) to a second electrical potential only once, namely directly at the rising clock edge following the precharging phase. After the rising clock edge, the state of the flip-flop input signal can no longer be altered. More particularly, changes in the input signal after the rising clock edge have no influence on the state of the flip-flop input signal generated by the pulse generator circuit. Accordingly, independent claims 29, 52 and 53, along with any dependent claims, are patentable over Matsuzaki for at least these reasons.

Additionally, as shown in Figure 45 of Matsuzako, NAND gate NA1 is part of a level-triggered flip-flop (*i.e.*, a latch) of a DRAM sense amplifier circuit. In contrast, the explicitly recited "pulse generator circuit" of amended claims 29, 52 and 53 is a component of an edge-triggered flip-flop that may, for example, be used as a synchronizing memory element where the synchronization occurs only at the rising clock edge. Additionally, the operation of the claimed edge-triggered flip-flop may clearly include three phases: (1) the flip-flop input signal is precharged to an electrical potential of a supply voltage ("precharge"); (2) the flip-flop input signal is brought to a second electrical potential and may be provided to the storage flip-flop subcircuit ("sample") at a rising clock edge; and (3) after the rising clock edge, the flip-flop input signal can no longer be altered and the storage flip-flop subcircuit holds the signal value ("hold").

Matsuzaki describes a latch with a level-triggered NAND gate (NA1), wherein the output of NA1 may be changed an arbitrary number of times (depending on the changing signal values of the input signals Ai and Aj) during a high level state of the timing signal ϕ. Matsuzaki, however, does not teach or suggest the circuit arrangement, and more particularly the edge-triggered flip-flop including a pulse generator circuit, required by amended claims 29, 52 and 53 as described above. As such, these amended independent claims are patentable over Matsuzaki.

With regard to claims 39-44, these claims have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuzaki in view of Sani et al. (U.S. Patent No. 6,794,914; hereinafter "Sani"). Each of these claims include all of the limitations of amended claim 29 by virtue of their dependence, and, therefore, these claims are patentable over the applied references for at least the reasoning discussed above with respect to independent claim 29. Applicants note that Sani is only cited for the additional limitations of these dependent claims, but does not cure the deficiencies of Matsuzaki. In particular, Sani neither discloses nor suggests an edge-triggered flip-flop or a pulse generator circuit as described above. Thus, amended claims 29, 52 and 53, along with claim 29's dependent claims, are novel over the prior art of record.

In view of the above remarks and amendments, Applicants submit that each of the presently pending claims in this application is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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